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A CMOS TRANSCONDUCTOR WITH ENHANCED LINEARITY AND TUNABILITY IN 0.18 µm TECHNOLOGY

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ABSTRACT

An enhanced configuration for a linearized MOS operational transconductance amplifier (OTA) is proposed. The proposed fully differential OTA circuit is based on feedback loops and passive components. It features high linearity, simplicity, and robustness against geometric and parametric mismatches. Detailed non-linearity analysis demonstrating the robustness of the proposed OTA is introduced. An efficient tuning technique using just a MOS transistor in the triode region allows the adjustment of the transconductance in a wide range. Simulation results of the transconductor designed in a 0.18 µm CMOS technology with 1.8 V supply confirm the high linearity predicted. The measured IM3 with an input voltage of 0.35 V Vpp is below 100 dB for the entire bandwidth of 53 MHz, and the input referred noise density is 65 nV/sqrtHz.

KEYWORDS: CMOS OTA, Harmonic Distortion, Linearity

INTRODUCTION

Fast arising technologies require higher circuit performances and this is the case for analog interfaces requiring active analog filters. Latest trend for communication systems is using more elaborated modulation schemes with higher data rates, which requires larger bandwidth and high linearity for the receiver front-end circuits and analog filters as well. For example, numerous types of multicarrier modulation schemes are used nowadays in many communication systems like asymmetric digital subscriber line (ADSL), very high bit-rate DSL (VDSL), 802.11 a/g wireless LANs, WiMax and digital video broadcasting (DVB). They are, in common, using multiple carriers over a wide bandwidth to provide robustness against the impairments of poor quality wireless and wired communication channels. These electronic systems require high linearity in a wide bandwidth to avoid intermodulation distortion among the multiple carriers. Thus, for example, ADSL requires a third-order intermodulation distortion (IM3) that is better than 60 dB in a signal band of 1.1 MHz, which extends to 4 MHz in ADSL2+ and up to 12 MHz in VDSL systems. Upcoming trends going toward higher data transfer rates will require higher frequency ranges with equal or better linearity.

When it is the concern of high frequencies, G_m-C technique which uses operational transconductance amplifiers (OTAs) or simply transconductance have observed to be the best candidate for the implementation of continuous time filters. Transconductance-C (G_m-C) filters usually feature higher operating frequencies. This advantage is arising from their open-loop operation. Furthermore, the transconductance can be tuned continuously allowing it to be flexible for filters of different specifications. The major disadvantage of OTAs is the large distortion caused by the nonlinear behavior of the transistors used. This problem results intermodulation terms at the output; this is the reason for the existence of a large number of reported techniques devoted to improve the linearity of OTAs and make it reached at the level comparable to RC topologies.

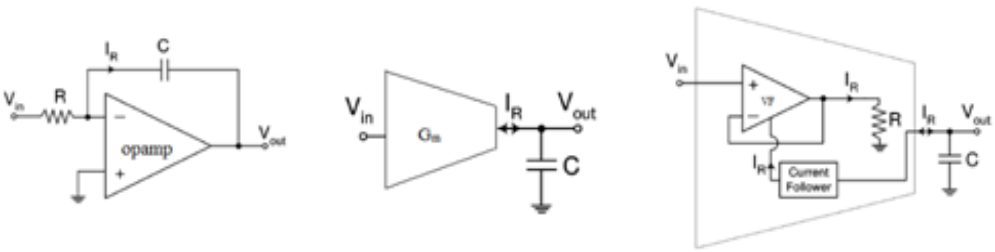
In this paper, a new topology is proposed which is a mixture of RC filter topology and G_m-C filter topology. It is well known fact that active RC filters exhibit better linearity than G_m-C filters at the cost of less bandwidth. This is because

active RC topologies follow the classic method for designing stable linear active circuits by means of feedback using passive linear elements. Linearity achieved in this way is very high as it depends on the voltage coefficient of the passive components as long as the gain of the active devices is high enough. G_m-*C* filters are known to achieve wideband operation and also less linearity, due to their open-loop operation.

HIGHLY LINEAR FILTER STRUCTURE

Whatever the topology we use in filter implementation, an integrator is always an essential part of it. Figure 1(a) shows this approach for an active RC integrator. A single-ended topology is shown for simplicity. It consists a passive resistor and a feedback capacitor. Resistor current is directly conveyed to the integrating capacitor.

Gm-C filters are known to achieve wideband operation and also less linearity, due to their open-loop operation. This fact makes *Gm-C* filters unusable for applications requiring very high linearity. To solve this problem, there have been several methods proposed by different authors to enhance the linearity of transconductance. But each of these methods has some disadvantages associated with it. So the basic trend is to use classic approach to achieve highly linear circuits, i.e., using feedback and passive resistors for implementing the transconductor, thus achieving a highly linear V–I conversion (e.g., [13]–[15]). Figure 1(b), (C) shows a G_m-C integrator following this approach. A feedback amplifier is used to implement a voltage follower that translates the input voltage to the resistor terminal, yielding a resistor current, like for the active integrator. The resistor current is typically made available at a high-impedance output node. However, to increase output voltage swing and/or to provide additional output impedance, a current follower is often employed to drive the integrating capacitor. The current follower senses an input current at its low impedance input and conveys it to its high-impedance output. Further, linearity can be improved by using differential configuration.



(a) **(b)** **(c)**

Figure 1: (a) RC Integrator (b) G_m-C Integrator (c) Linear G_m-C Integrator

Continuous tuning of the transconductance value is usually required in continuous time G_m-C filters to compensate for RC process variations. Typically, a tuning range of about 50% is required for this task. Even if the transconductor features high linearity, an inefficient tuning strategy may partially waste it. Hence, the inclusion of tuning should minimize the degradation of linearity and, at the same time, preserve the performance of the transconductor (input range, bandwidth, etc.). A tuning method, shown in Figure 2, employs a resistive divider to split the output current, thus leading to current attenuation. If resistors are made programmable, attenuation can be adjusted. Despite the fact that tuning is based on adjusting resistance values, the method has important advantages. First, tunable resistors do not modify the V-I conversion core. Second, tuning accuracy depends on ratios of resistors and not on the absolute value of a resistor. This makes tuning more linear and less dependent on thermal and process variations. In addition, since tuning does not rely on the absolute value of the tuning resistors, tuning resistances can be made small so that voltage swing at the terminals of the tuning resistors is minimized. Hence, they lead to less distortion as compared with tuning the V-I. conversion resistor in the transconductor or in a MOSFET- filter, which experiences the full input-signal swing. After introducing tuning scheme transconductance circuit is shown in figure (3).

Transconductance of the circuit can be given as:

$$G_m = \frac{\alpha I_R}{V_{id}} \quad (1)$$

Where $V_{id} = V_{i+} - V_{i-}$ and αI_R is output current of current follower.

Current is splited by current divider circuit by a factor α which can be calculated as:

$$\alpha = 1 \Big/ \left(1 + \frac{R_2}{R_1}\right)$$

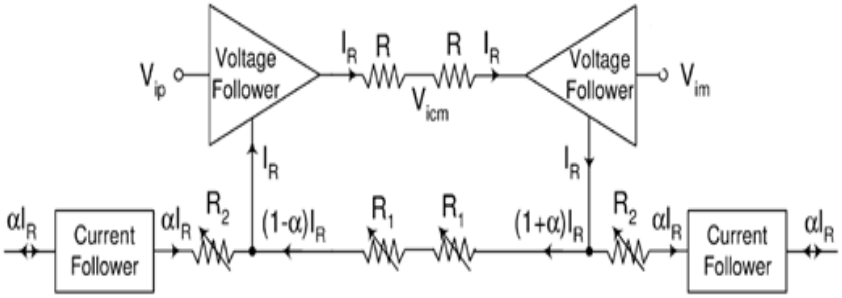


Figure 2: Linear Transconductor with Tuning Scheme

TRANSCONDUCTOR CIRCUIT IMPLEMENTATION

After going through the analysis in previous sections, a new programmable transconductor that represents high linearity and good trade-offs between power and circuit simplicity is implemented in this section. The voltage follower chosen is based on servo loop technique, which features simple implementation, faster and power efficient with highly linear behavior. Current follower is the folding stage which is also simple to design and exhibits good insensitivity to transistor mismatch. A very simple tuning scheme is proposed, requiring only one transistor in the triode region, which is based on a modification of the scheme in Figure 2.

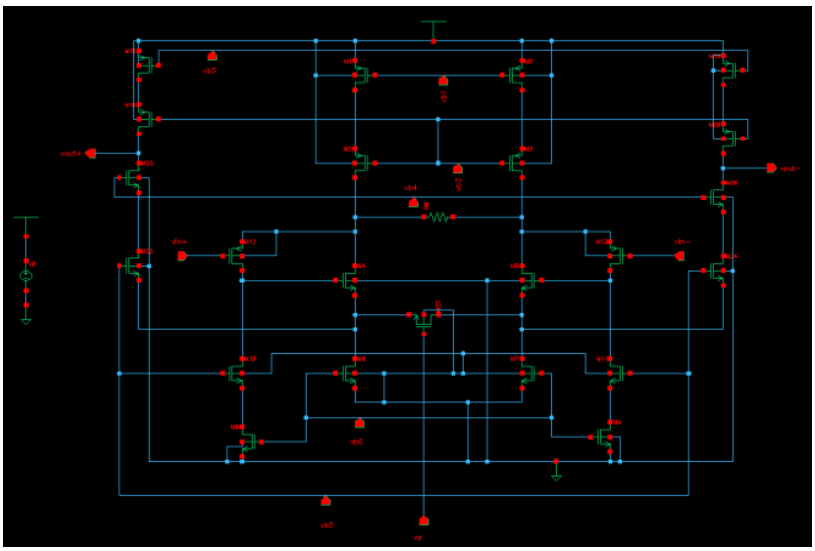


Figure 3: Schematic of Transconductor

The detailed schematic of the transconductor is shown in Figure 3. All bias currents are equal. Cascode current sources are employed when high output resistance is required.

Since the programming transistor leads to a decrease in output resistance which is also dependent on tuning, an additional cascode transistor M_{CN2} has been included. To improve linearity, pMOS input transistors have been embodied in

independent wells connected to their respective sources, as shown in Figure 3. This leads to a bulk-to-substrate capacitance which is approximately at few of few fF. This capacitance can create a zero in the transconductance. However, for the frequency range and low factor of the filter presented in the next section, this capacitance was not relevant.

SIMULATION RESULTS

Proposed transconductor is implemented in CADENCE tool using virtuoso schematic editor. The dc transfer characteristics of voltage follower and current follower are shown in Figure 4 and Figure 5. Both the characteristics fulfill expected linear operation of subsections of proposed circuit. **:** DC transfer characteristics of proposed OTA is shown in figure 6.While performing this analysis, V_{in-} is kept at 350mV and $V_{in}+$ is swept through the range 0-700mV. Output nodes are terminated by 1KΩ resistor while performing this analysis. Different values of differential output currents for different values of programming voltage V_p are also superimposed in the graph.

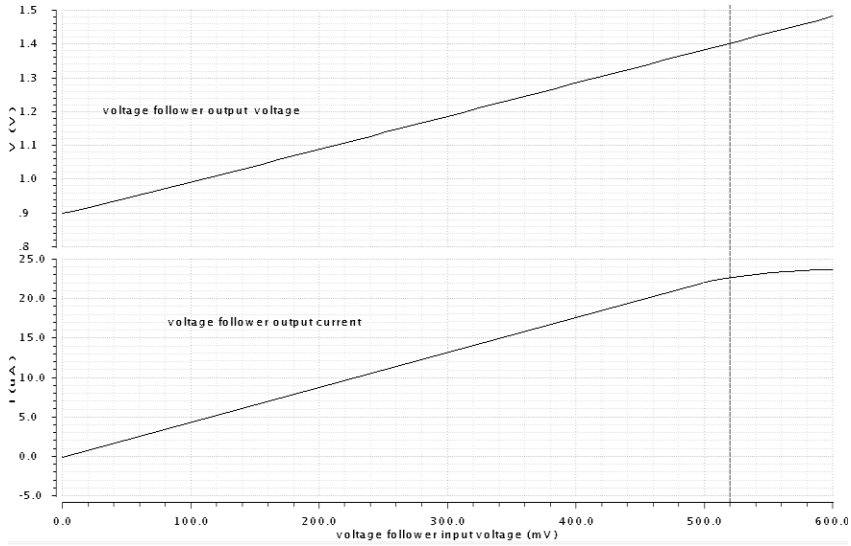


Figure 4: DC Transfer Characteristics of Voltage Follower

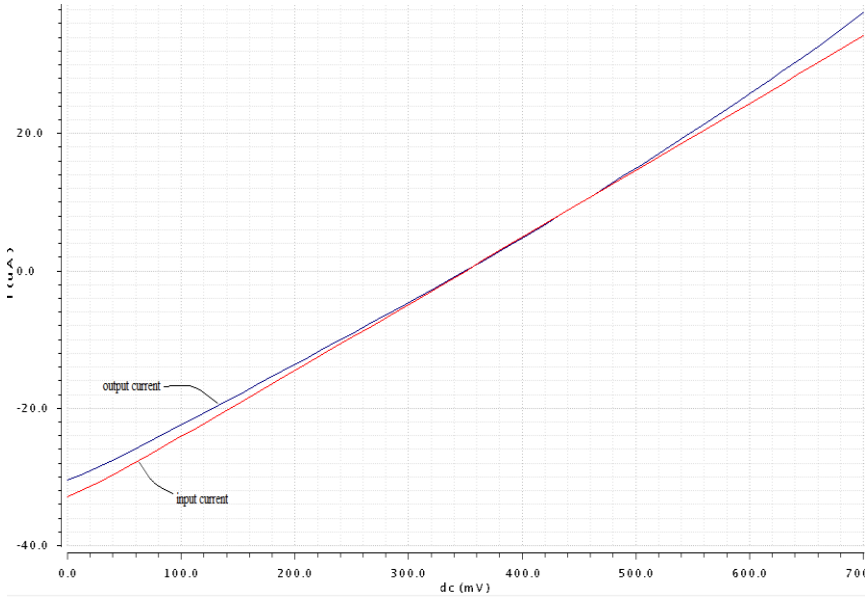


Figure 5: DC Transfer Characteristics of Current Follower

At any value of input voltage transconductance of the circuit can be given as:

$$G_m = \frac{I_{out+} - I_{out-}}{V_{in+} - V_{in-}}$$

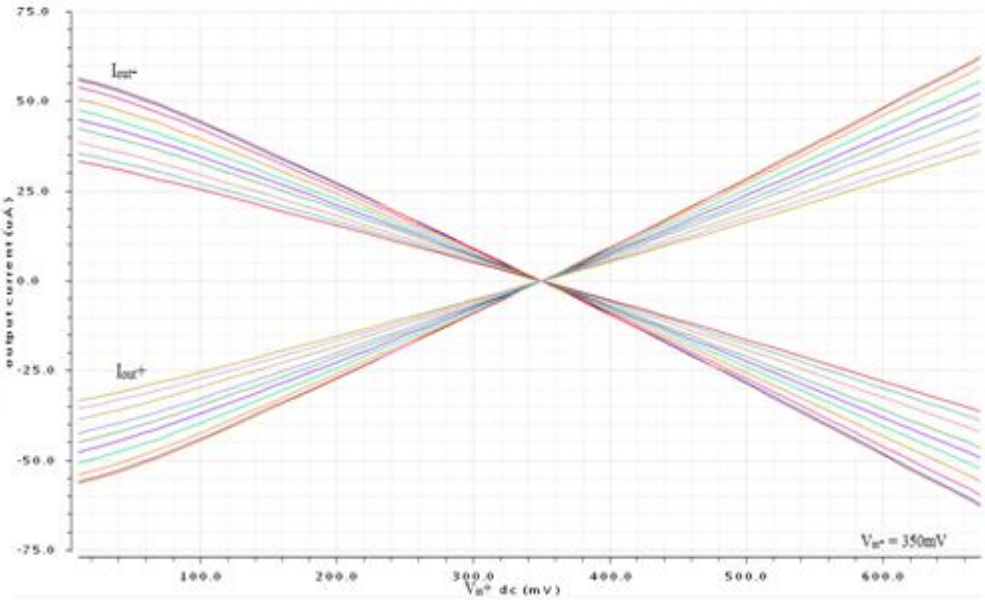


Figure 6: DC Transfer Characteristics of Transconductor

By observation of graph,

$$\text{maximum } G_m = \frac{61\,\mu A-(-61\,\mu A)}{0-(-350\,mV)} = 348\,\mu A/V$$

$$\text{minimum } G_m = \frac{32\,\mu A-(-32\,\mu A)}{0-(-350\,mV)} = 182.8\,\mu A/V$$

$$\text{percentage tuning of } G_m = \frac{348-182.8}{348} \times 100 = 47.4\%$$

Thus 47.4% tuning range is achieved which is a good figure for any tuning scheme.

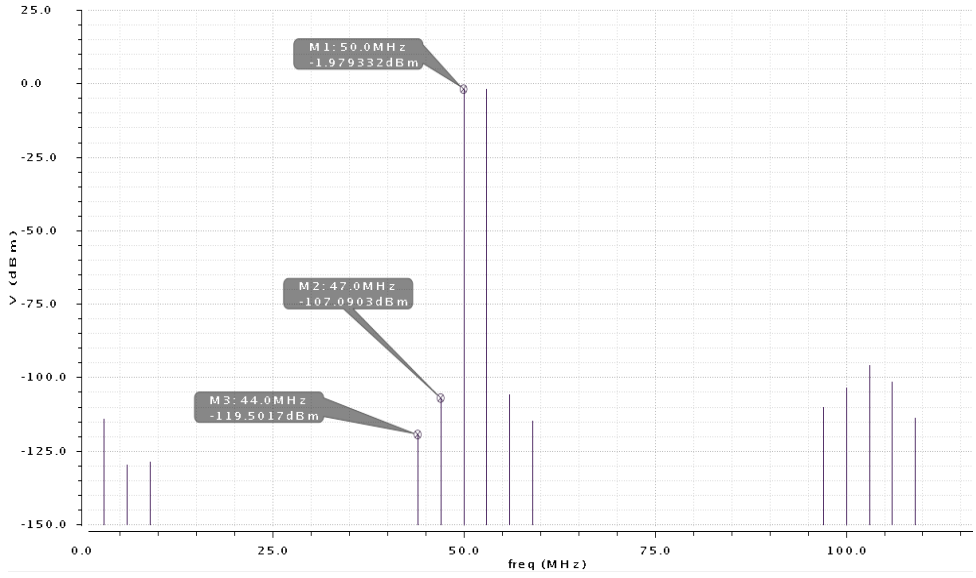


Figure 7: IM3 Distortion Calculation

A two tone analysis is done for IM_3 distortion calculation. A sinusoidal input signal with two harmonics of ω_1=50 MHz and ω_2=53 MHz is applied. Port resistances are set to the value of 50 Ohms. Third order harmonics 47 MHz and 56 MHz are also present in the output of circuit. Related simulation graph is shown in figure 6.7. Output voltage correspond to 50 MHz and 47 MHz is observed as -1.97 dBm and -107 dBm respectively. IM3 product is the difference of these two voltage levels i.e. -105.03 dBm. This figure shows tremendous linearity performance by the circuit.

Thus, the results discussed so far reflect overall behavior of proposed transconductance. A summary of simulated results is mentioned in table 1.

Table 1: Summary of Simulated Results

Specification	Value/Range
Technology	0.18 µm CMOS
Power supply	1.8 V
Bias current	75 µA
G_m tuning range	348-182.8 µA/V
Percentage G_m tuning	47.4%
Differential AC gain	41 dB
Bandwidth	53.33 MHz
IM3 @50MHz	-105.12 dB
CMRR @50MHz	63.32dB
Input referred noise @1MHz	$65\ nV/\sqrt{Hz}$
Power consumption	0.54 mW

CONCLUSIONS

A simple and highly linear transconductor has been proposed. Linearity has been achieved by adapting usage of feedback loops and passive components as in the case of circuits based on RC filter topology. Circuit was made fully differential in order to suppress second order terms causing non-linearity. Voltage to current conversion was achieved by connecting resistive load at the output of a voltage follower. Output impedance has been increased by inserting a current follower at the output. The circuit is nearly insensitive to transistor mismatch.

Simulation results of the transconductor show an IM3 of 105 dB for a two-tone 0.35-V_{pp} input signal at 50 MHz which witness to sound achievement of the circuit in terms of linearity. 41 dB constant differential gain upto 50 MHz is also adaptable in nature in many high frequency G_m-C filters used in communication systems. Transconductance with approximately 50% programmability is a bright feature of tuning scheme.

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